

Limits of Uneven Battery Power in Modular Multilevel Converter-based Battery Energy Storage Systems

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Abstract—For modular multilevel converter-based battery energy storage systems (MMC-BESS), uneven power among batteries of SMs will be deduced by battery aging, battery fault, etc., which will degrade performance and even lead to system failure. For maintaining the balance of capacitor voltage, this paper analyzes the limits of the uneven power of batteries, which are presented as the current limits in this paper. According to analysis, an analytical method is proposed that only the dc and fundamental frequency components of the arm current are used to calculate current limits. With the current limits it is able to evaluate the reasonability of power distribution among batteries. Meanwhile, increase of fundamental frequency component will enhance the current limits, and the dc component determines the size relationship between the absolute values of the upper and lower current limits. Finally, simulation model and experiment prototype are built for verifying the theoretical analysis and current limits calculation method, and satisfactory results are provided.

Index Terms—Arm current, balance of capacitor voltage, current limits, MMC-BESS, uneven power.

I. INTRODUCTION

MODULAR multilevel converter (MMC) was originally applied in the field of high-voltage direct current (DC) power transmission [1], [2]. With the efforts of continuous research and exploration, MMC has gained extensive attention in applications of medium/high voltage due to its advantages of modularity, low harmonic, and low switching frequency [3]–[5]. Recent studies [6], [7] have introduced the MMC to energy storage system (ESS) applications, especially for battery energy storage system (BESS) which is one of the most attractive ESS alternatives [8], [9]. Taking the advantage of modularity of MMC, each battery of BESS is connected to a submodule (SM) by a bidirectional DC-DC converter. Fig. 1(a) shows the circuit diagram of a single-phase MMC-BESS.

Manuscript received March 3, 2021; revised June 24, 2021; accepted August 17, 2021. Date of online publication September 5, 2022; date of current version July 31, 2023. This work was supported by Key Research and Development Program of Hebei Province under Grant 19214405D, and National Natural Science Foundation of China under Grant 51677162.

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DOI: 10.17775/CSEEJPES.2021.01510

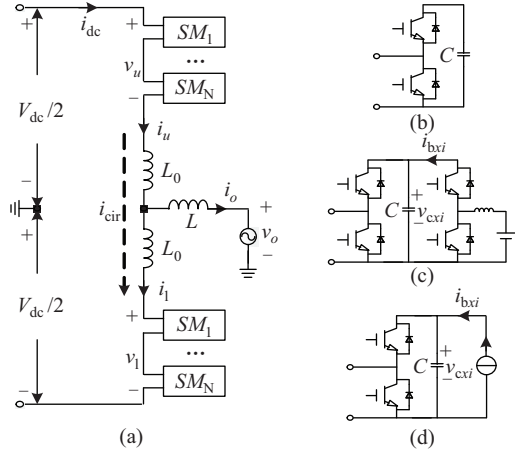


Fig. 1. Diagram of a single phase MMC-BESS: (a) single phase MMC-BESS, (b) half-bridge SM, (c) half-bridge SM with battery, (d) half-bridge SM with parallelly connected current source.

Each arm consists of N SMs and an arm inductor. Standard SM (SSM) of MMC, as shown in Fig. 1(b), contains a half bridge and a capacitor. Fig. 1(c) shows an SM integrated with a battery (BSM) through a chopper circuit. To avoid conceptual confusion, in this paper, SSM and BSM are used to refer to the SM without or with the battery unit separately. The scheme of MMC-BESS features low battery voltage, and high reliability of BESS as the fault of one battery merely affecting the connected submodule [10]. Meanwhile, MMC-BESS is capable of directly managing power flows among the alternating current (AC) bus, high voltage DC bus and BESS without additional intermediate power conversion stages.

In an MMC-BESS, battery aging, battery fault, combinations of SSM and BSM in one arm and so on, will deduce uneven average power transmission [11]–[15]. For an example, [11] focused on the condition of battery faults the faulty battery units are unable to exchange active powers with AC or DC ports and [12] considered the hybrid combination of SSM and BSM in each arm. For the battery unit, balancing state of charge (SoC) [13], [14] and state of health (SOH) [15] among batteries are studied. The corresponding control scheme for power transmission among the AC port, DC port and battery units was carried out in these literatures.

Furthermore, the unbalanced battery unit also disturbs power balances of inter-leg, inter-arm and submodules of the

MMC-BESS, thus degrading performance and even leading to system failure. Impacts of uneven battery power of BSMs on power balances of inter-arm and inter-leg could be eliminated by regulating the dc and fundamental frequency components of circulating currents of each phase [16], [17].

This paper will focus on the influences of uneven battery power of BSMs on the balance of capacitor voltage of BSMs, and in this field [18]–[21] have done lots of interesting works. References [18]–[20] studied the number limits of BSMs that could maintain the power balance of MMC-BESS and capacitor voltage balance. However, in [18], [19], batteries in BSMs provide the same power, which is a special case of uneven battery power of BSMs and is lack of generality. Though it is referred in [20] the batteries of BSMs can provide uneven power, it is a lack of further research about the impacts of uneven battery power of BSMs on capacitor voltage balance.

From the perspective of research methods, a graphical method was proposed in [18] and it is difficult to evaluate system stability in real-time. A numerical method was presented in [19] while only the power flow between AC port and BSM is considered. Analytical and numerical methods were illustrated in [20]. The analytical method could simplify the analysis while introducing significant errors as noted by the authors. The numerical method improves accuracy, yet computational consumption is considerable.

An analysis about the influences of an arbitrary distribution of battery power of BSMs on the balance of capacitor voltage was conducted in [21]. A method that calculates the power limits of batteries was proposed. A criterion vector of N -1 dimension and a criterion value were proposed to determine the reasonability of an uneven power distribution of batteries. However, each vector element needs to integrate power injected from the MMC to SMs during a fundamental frequency period, and vector dimension is proportional to the total number of SMs. Computational consumption of the proposed method would increase along with the increment of the number of SMs, and will be considerable when N is large.

With the power balance of MMC-BESS, power limits are presented as the limits of current which is injected by the connected bidirectional converter to the SM. Aiming to the balance of capacitor voltage, an analytical method is proposed in this paper, which only utilizes the dc and fundamental frequency components of the arm current to calculate current limits. With current limits, it is able to evaluate reasonability of the power distribution among batteries. Computational consumption of the proposed method is fixed and independent of the number of SM and SMs within one arm responding to the same current limits.

The rest of this paper is organized as follows. The basic relationships of currents of MMC-BESS and BSM capacitor model are introduced in Section II. Section III analyzes the critical states and derives the current limits calculation method. Simulation and experimental results are provided in Section IV and Section V, respectively. Finally, Section VI summarizes the main conclusions of this paper.

II. BASIC FEATURES OF MMC-BESS

In Fig. 1, V_{dc} and i_{dc} represent DC side voltage and current, respectively. L_0 and L are arm inductor and AC side inductor. AC side voltage and current are represented by v_o and i_o . The number of SM within one arm is N . v_x and i_x ($x = u, l$) are the arm voltage and current, respectively, where u and l represent the upper and lower arms. i_{cir} is the circulating current that flows through the phase leg. SM capacitance is C . v_{cxi} is the capacitor voltage and i_{bxi} represents the current from the bidirectional converter to SSM, where the subscript i represents the i -th SM in the upper or lower arm. In this paper, the phase-disposition pulse width modulation (PD-PWM) and sorting algorithm are used to balance capacitor voltage [22]. In order to simplify analysis, the battery and bidirectional converter in BSM are regarded as a current source [23], [24] connected in parallel with the SSM capacitor, as shown in Fig. 1(d).

The basic principle of MMC-BESS has been discussed in [16] and [18] and this section only discusses the relationships among the arm currents, circulating current and AC side current to make a foundation for subsequent analysis. Fig. 2 is the equivalent circuit of the single phase MMC-BESS in Fig. 1(a). P_{bu} is total battery power in the upper arm and P_{bl} is total battery power in the lower arm.

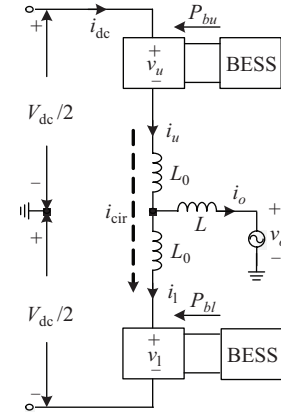


Fig. 2. Equivalent circuit of the single phase MMC-BESS.

Utilizing Kirchhoff's current law in Fig. 2, arm currents are

$$\begin{cases} i_u = i_{cir} + \frac{i_o}{2} \\ i_l = i_{cir} - \frac{i_o}{2} \end{cases} \quad (1)$$

Assuming v_o and i_o are

$$\begin{cases} v_o = V_o \sin(\omega t) = \frac{V_{dc}}{2} m \sin(\omega t) \\ i_o = I_o \sin(\omega t + \theta) \end{cases} \quad (2)$$

where V_o and I_o are AC side voltage and current peak values. m is the modulation ratio. ω is the fundamental angle frequency, and θ is the power factor angle.

Assuming the capacitors of SMs are large enough to absorb the second harmonic component of circulating current, the

phase leg circulating current i_{cir} including dc and fundamental frequency component is represented as

$$i_{\text{cir}} = I_{\text{cir}} + I_{\text{cir}1} \sin(\omega t + \varphi) \quad (3)$$

where I_{cir} represents the dc component of circulating current, and equals to the dc component of i_{dc} in the single phase MMC-BESS. $I_{\text{cir}1}$ is the amplitude of fundamental frequency component. φ is the phase angle between v_o and the fundamental frequency component of circulating current.

Substituting (2) and (3) into (1), arm currents i_u and i_l are

$$\begin{cases} i_u = I_{\text{cir}} + I_{u\text{arm}} \sin(\omega t + \varphi_u) \\ i_l = I_{\text{cir}} + I_{l\text{arm}} \sin(\omega t + \varphi_l) \\ I_{u\text{arm}} = \sqrt{I_{\text{cir}1}^2 + I_o^2/4 + I_{\text{cir}1} I_o \cos(\theta - \varphi)} \\ I_{l\text{arm}} = \sqrt{I_{\text{cir}1}^2 + I_o^2/4 - I_{\text{cir}1} I_o \cos(\theta - \varphi)} \end{cases} \quad (4)$$

where φ_u is the phase angle between i_u and v_o , and φ_l is the phase angle between i_l and v_o . $I_{u\text{arm}}$ and $I_{l\text{arm}}$ are amplitudes of fundamental frequency component of upper and lower arm currents.

III. ANALYSIS OF BSM CURRENT LIMITS

A. Analysis of Critical States

Figure 3 is the circuit diagram of BSM_{xi} and S_{cxi} is the switching function of BSM_{xi} . S_{cxi} represents the insert/bypass state of BSM_{xi} , which are illustrated as 1 and 0, respectively. When switch S_1 is on and switch S_2 is off, BSM_{xi} is inserted and $S_{cxi} = 1$. Similarly, when switch S_1 is off and switch S_2 is on, BSM_{xi} is bypassed and $S_{cxi} = 0$.

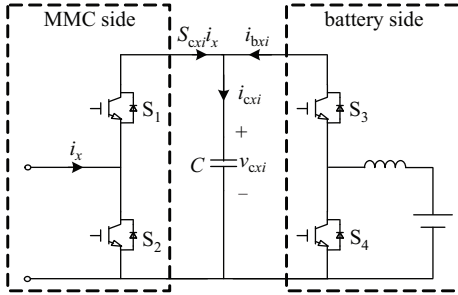


Fig. 3. Circuit diagram of BSM_{xi} .

For each arm, the required number of SMs to be inserted is n_x , which is determined by PD-PWM. To accomplish the task of the capacitor voltage balance of SMs in each arm, a sorting algorithm is adopted. In the sorting algorithm, SM capacitor voltages of each arm are measured and sorted, first. Then, if the current of upper (lower) arm is positive, n_x of the SMs with lowest voltages are identified and inserted. The S_{cxi} of the corresponding SMs are set to 1 and corresponding capacitors are charged. If the current of upper (lower) arm is negative, n_x of the SMs with highest voltages are identified and inserted. S_{cxi} of the corresponding SMs are set to 1 and corresponding capacitors are discharged. Regardless of the direction of the arm current, the rest of the SMs will be bypassed and the corresponding S_{cxi} is set to 0.

As illustrated in Fig. 3, capacitor voltage in a BSM is determined by the arm current, the switching function of BSM and the current i_{bxi} , which can be described as

$$C \frac{dv_{cxi}}{dt} = S_{cxi} i_x + i_{bxi} \quad (5)$$

As zero average net power of BSM capacitor has to be maintained during a fundamental period T , variation of BSM capacitor voltage is zero within a period of T .

$$\int_0^T C \frac{dv_{cxi}}{dt} dt = \int_0^T S_{cxi} \cdot i_x dt + \int_0^T i_{bxi} dt = 0 \quad (6)$$

Equation (6) illustrates that to maintain the capacitor voltage stability within a period of T , the sum of the charges provided by arm current i_x and the current i_{bxi} has to be zero.

According to (6), zero net charge within a period of T is required to keep BSM capacitor voltage constant, thus arm current i_x should follow with variation of i_{bxi} . Meanwhile, adjustment of switching function S_{cxi} based on sorting algorithm is also important.

Define $\alpha = I_{\text{cir}}/I_{x\text{arm}}$, and the waveforms of arm current i_x , shown in Fig. 4, contain different features according to the variation range of α . As shown in Fig. 4(a) and (e), i_x has only one polarity (positive or negative) which can just provide positive (negative) charges to balance negative (positive) charges from i_{bxi} . For i_x in Fig. 4(b), (c) and (d), each case contains currents of two polarities (positive and negative) and is capable of providing charges to balance both positive and negative charges provided by i_{bxi} .

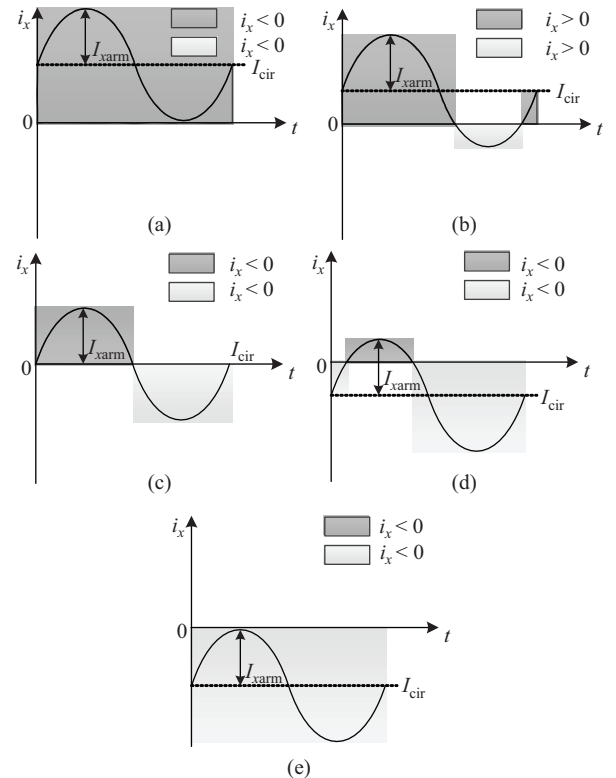


Fig. 4. Waveforms of the arm current i_x with different α : (a) $\alpha \geq 1$, (b) $0 < \alpha < 1$, (c) $\alpha = 0$, (d) $-1 < \alpha < 0$ and (e) $\alpha \leq -1$.

According to (6), (7) defines Q_{Tx} as charges provided by i_x within a period of T .

$$Q_{Tx} = \int_0^T S_{cxi} \cdot i_x dt = - \int_0^T i_{bxi} dt \quad (7)$$

In (7), it is obvious S_{cxi} is able to adjust Q_{Tx} . Therefore, S_{cxi} may have two kinds of critical states with a certain i_x as shown in Fig. 5, which takes the arm current with $0 < \alpha < 1$ as an example to analyze the critical states.

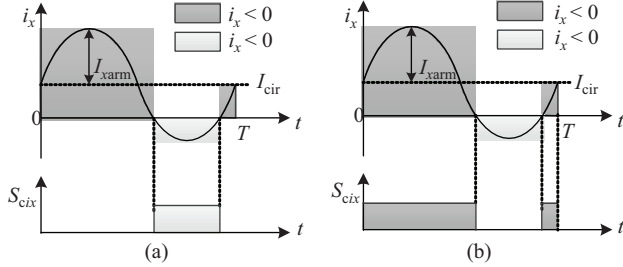


Fig. 5. Critical states of i_x with $0 < \alpha < 1$: (a) S_{cxi} is on only during $i_x \leq 0$, (b) S_{cxi} is on only during $i_x > 0$.

Critical state a (Fig. 5(a)): if S_{cxi} is on only during the period of $i_x \leq 0$, i_x can provide maximum negative charges to BSM capacitor at the end of the period in this condition, denoted as $Q_{Tx_min} < 0$.

$$Q_{Tx_min} = \int_0^T S_{cxi} i_x dt$$

$$S_{cxi} = \begin{cases} 1 & i_x \leq 0 \\ 0 & i_x > 0 \end{cases} \quad (8)$$

Critical state b (Fig. 5(b)): if S_{cxi} is on only during the period of $i_x > 0$, i_x can provide maximum positive charges to BSM capacitor at the end of the period in this condition, denoted as $Q_{Tx_max} > 0$.

$$Q_{Tx_max} = \int_0^T S_{cxi} \cdot i_x dt$$

$$S_{cxi} = \begin{cases} 0 & i_x \leq 0 \\ 1 & i_x > 0 \end{cases} \quad (9)$$

Observing Fig. 4 and considering the critical states, i_x owns two critical states (a and b) when α belongs to $(-1, 1)$. When $\alpha \leq -1$, i_x only satisfies the condition of critical state a. Similarly, when $\alpha \geq 1$, i_x only satisfies the condition of critical state b.

B. Derivation of Current Limits

Define I_{baxi} as the average current of current source i_{bxi} in period of T .

$$I_{baxi} = \frac{1}{T} \int_0^T i_{bxi} dt \quad (10)$$

where the subscript a represents the average value.

When I_{baxi} is positive, charges of i_x should be negative for stabilizing BSM capacitor voltage. Negative charges of i_x increases following the increase of I_{baxi} until S_{cxi} operates at the critical state a. When I_{baxi} increases further, adjusting

S_{cxi} is unable to maintain establishment of (6). Therefore, maximum positive current I_{baxi} is obtained at critical state a, denoted as the upper current limit I_{bax_max} . Substituting (8) and (10) into (7), I_{bax_max} is

$$I_{bax_max} = - \frac{Q_{Tx_min}}{T} \quad (11)$$

Similarly, critical state b corresponds to maximum negative current, denoted as the lower current limit I_{bax_min} . Substituting (9) and (10) into (7), I_{bax_min} is

$$I_{bax_min} = - \frac{Q_{Tx_max}}{T} \quad (12)$$

Substituting (4), (8), (9) into (11) and (12), current limits equations are different with different range of α .

When $\alpha \geq 1$, the current limits are

$$\begin{cases} I_{bax_max} = 0 \\ I_{bax_min} = -I_{cir} \end{cases} \quad (13)$$

When $\alpha \leq -1$, current limits are

$$\begin{cases} I_{bax_max} = -I_{cir} \\ I_{bax_min} = 0 \end{cases} \quad (14)$$

When $-1 < \alpha < 1$, current limits are

$$\begin{cases} I_{bax_max} = I_{cir} \frac{\Delta t}{T} + \frac{\sqrt{I_{xarm}^2 - I_{cir}^2}}{\pi} \\ I_{bax_min} = I_{cir} \frac{-\Delta t - T}{T} - \frac{\sqrt{I_{xarm}^2 - I_{cir}^2}}{\pi} \end{cases} \quad (15)$$

where

$$\Delta t = \frac{2 \arcsin(\alpha) - \pi}{\omega}$$

According to the derivation above, the current limits are decided by the arm current. As the SMs within one arm are connected in series and share the same arm current, it is the same for current limits of SMs within one arm. The flowchart for calculating current limits and judging the balance of capacitor voltage is shown in Fig. 6. It is obvious that only one loop is required to directly obtain current limits. Therefore, the computational consumption of the proposed method is fixed and independent on the number of SM.

C. Current Limits Characteristic Analysis

According to (13)–(15), the sum of current limits is expressed as

$$I_{bax_max} + I_{bax_min} = -I_{cir} \quad (16)$$

From (16), the sum of current limits is determined by I_{cir} . Therefore, if one current limit (upper or lower limit) is calculated, the other one can be obtained according to (16).

Figure 7 shows the relationships of current limits versus I_{xarm} and I_{cir} . When $\alpha \geq 1$, I_{bax_min} equals $-I_{cir}$, and I_{bax_max} is a constant zero. Similarly, when $\alpha \leq -1$, I_{bax_min} is a constant zero, and I_{bax_max} is $-I_{cir}$. A constant zero means imbalance among BSMs capacitor voltages will happen, on the conditions of a positive I_{baxi} when $\alpha \geq 1$ and a negative I_{baxi} when $\alpha \leq -1$.

With $-1 < \alpha < 1$ and fixed I_{xarm} , I_{bax_max} gradually decreases from $-I_{cir}$ to zero following the increase of I_{cir} .

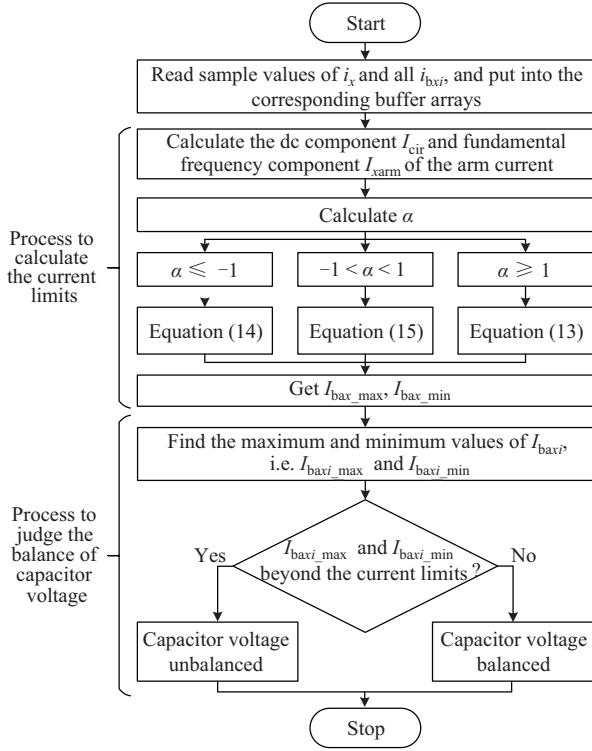


Fig. 6. The flowchart for calculating the current limits and judging the balance of capacitor voltage.

Reversely, I_{bax_min} gradually increases from zero to $-I_{cir}$ following the increase of I_{cir} . Considering the absolute value, I_{bax_max} is larger than I_{bax_min} when $I_{cir} < 0$ and I_{bax_max} is less than I_{bax_min} when $I_{cir} > 0$.

With a fixed I_{cir} , absolute values of the upper and lower current limits increase along with increase of I_{xarm} . Particularly, when dc current is zero, that is, $I_{cir} = 0$, current limits are simplified to the same absolute value with opposite signs, expressed as

$$\begin{aligned} I_{bax_max}|_{I_{cir}=0} &= \frac{I_{xarm}}{\pi} \\ I_{bax_min}|_{I_{cir}=0} &= -\frac{I_{xarm}}{\pi} \end{aligned} \quad (17)$$

In summary, I_{xarm} is responsible to the range of current limits. I_{cir} determines the sum of the upper and lower current limits. The sign of I_{cir} determines the relative size between the absolute values of the upper and lower current limits.

In (4), the dc components of upper and lower arm within one phase leg are the same while amplitudes of fundamental frequency component may differ as the existence of fundamental frequency component of the circulating current. Thus, the current limits of the upper and lower arms may be different when circulating current contains the fundamental frequency component.

According to (4), I_{uarm} and I_{larm} are both $I_o/2$ when $I_{cir1} = 0$. When $I_{cir1} \neq 0$, I_{uarm} and I_{larm} may differ. Define $\beta = 2I_{cir1}/I_o$, and select $I_o/2$ as the base value. Equation (4) can be simplified as

$$\begin{cases} I_{uarm}^* = \sqrt{\beta^2 + 1 + 2\beta \cos(\theta - \varphi)} \\ I_{larm}^* = \sqrt{\beta^2 + 1 - 2\beta \cos(\theta - \varphi)} \end{cases} \quad (18)$$

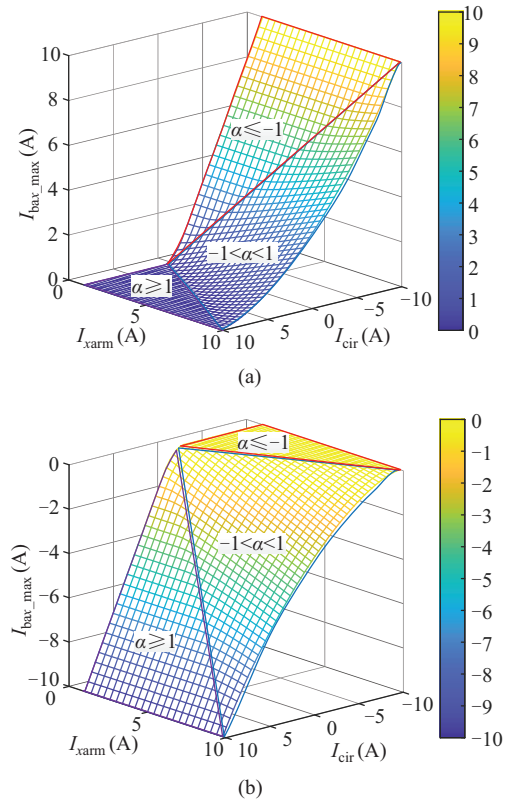


Fig. 7. Relationships of current limits vs I_{xarm} & I_{cir} : (a) I_{bax_max} vs I_{xarm} & I_{cir} , and (b) I_{bax_min} vs I_{xarm} & I_{cir} .

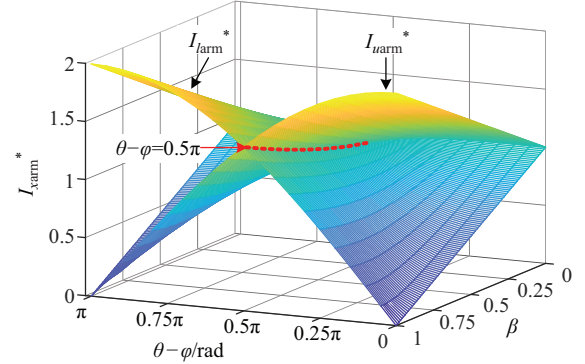


Fig. 8. Relationship of I_{xarm}^* vs β and $(\theta - \varphi)$.

According to (18), Fig. 8 shows the relationship of the amplitudes of fundamental frequency component of arm currents versus β and $(\theta - \varphi)$.

In Fig. 8, I_{uarm}^* and I_{larm}^* are symmetrical about $(\theta - \varphi) = \pi/2$. When $(\theta - \varphi) = \pi/2$, that is, i_{cir1} is perpendicular to i_o , I_{uarm}^* and I_{larm}^* are equal to each other and increase following increase of β .

When $0 < (\theta - \varphi) < \pi/2$, $I_{uarm}^* > I_{larm}^*$. With increase of β , I_{uarm}^* gradually rises and I_{larm}^* gradually falls. As $(\theta - \varphi)$ increases, I_{uarm}^* gradually decreases and I_{larm}^* gradually increases. In addition, it is obvious that I_{uarm}^* is always greater than I_{larm}^* . Thus, in the range of $0 < (\theta - \varphi) < \pi/2$, the current limit range of upper arm is larger than of lower arm.

When $\pi/2 < (\theta - \varphi) < \pi$, it is similar to that of $0 < (\theta - \varphi) < \pi/2$.

IV. SIMULATION VERIFICATION

In order to verify analysis of the current limits, a simulation model of a single phase MMC-BESS, as shown in Fig. 1, is built and simulation parameters are shown in Table I.

For validating the analysis of the current limits, the whole system control diagram is shown in Fig. 9. AC side voltage is controlled with a PI controller and a sorting method is adopted to balance capacitor voltages. For maintaining balance between the arm voltages, a circulating current control strategy with PIR controller is used, and the detailed diagram is in Fig. 10. v_{cu} and v_{cl} are the sum of the SM capacitor voltages on the upper and lower arms, respectively. Parameters of the controllers in simulation system are shown in Table II.

For a simplified description, the current of the current source in BSM is called the current of BSM for short.

TABLE I
SIMULATION PARAMETERS OF MMC-BESS

Parameter	Value
Amplitude of AC voltage/ V_o (V)	2000
Amplitude of AC current/ I_o (A)	200
DC voltage/ V_{dc} (V)	5000
Number of BSM per arm/N	5
BSM capacitor voltage/ V_c (V)	1000
BSM capacitance/ C (mF)	5
Arm inductor/ L_0 (mH)	5
AC inductor/ L (mH)	3
Fundamental frequency (Hz)	50

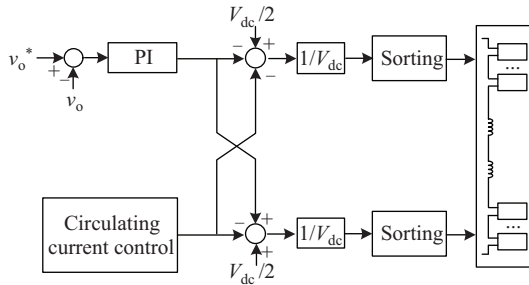


Fig. 9. Diagram of the system control strategy.

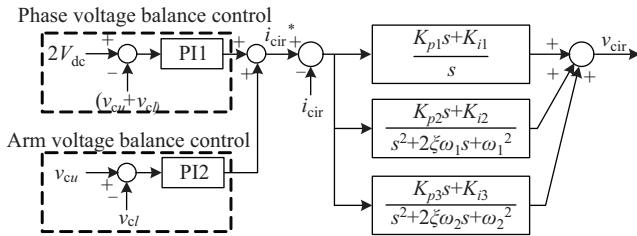


Fig. 10. Diagram of the circulating current control.

TABLE II
PARAMETERS OF CONTROLLERS IN SIMULATION SYSTEM

Parameter	Value	Parameter	Value
K_p in PI	0.2	K_{p1}	3
K_i in PI	0.001	K_{i1}	0.01
K_p in PI1	2	K_{p2}	10
K_i in PI1	0.001	K_{i2}	1
K_p in PI2	0.1	K_{p3}	80
K_i in PI2	0.0001	K_{i3}	0
ζ	0.05		

A. Case I

Initially, AC port power is supplied solely by the DC port and currents of all BSMs are set to zero. Utilizing parameters exhibited in Table I, current limits in upper arm can be calculated as $I_{bau_max} = 14.4$ A and $I_{bau_min} = -39.8$ A. Currents of all BSMs are within the current limits and capacitor voltages are balanced as shown in Fig. 8(a).

At 0.3 s, currents of SM1 and SM2 in the upper arm are changed to 14 A and -14 A, respectively. As total power provided by batteries in the upper arm is unchanged, arm current of upper arm is unchanged and current limits stay the same. Currents of SM1 and SM2 still remain the current limits and capacitor voltage balance is maintained.

At 0.6 s, currents of SM1 and SM2 change to 15 A and -15 A. Current limits remain unchanged while the current of SM1 is beyond the upper current limit. Thus, capacitor voltage of SM1 deviates from the other BSMs, as analyzed in Section II.

Figure 11(b) and (c) are the detailed waveforms of the upper arm current and driving signals of SM1 to SM5 around 0.3 s and 0.6 s. At 0.3 s, current of SM1 is about to go beyond the upper current limit and the driving signal of SM1 is closed to critical state a. Though inserted during the whole period of $i_u < 0$, SM1 still has insert-states within $i_u > 0$ as shown in Fig. 11(b). At 0.6 s, the current of SM1 is beyond the upper current limit and the driving signal of SM1 keeps in critical state a. However, i_u could not provide enough negative charges for the capacitor which leads to deviation of SM1 capacitor voltage.

B. Case II

This case is to verify the change of current limits with fixed $I_{xarm} = 200$ A and changed I_{cir} , in simulation. In this case, BSMs in the upper arm are the same as BSMs in the lower arm, and the upper arm is taken as an example to be analyzed.

Initially, as shown in Fig. 12, currents of SM1 and SM2 are set to 15 A and -15 A, and the other BSMs are set to zero. The initial condition of this case is the same as the condition between 0.6 s and 1 s of Case I. Therefore, BSMs in the upper arm are imbalanced, the same as in Fig. 11.

At 0.6 s, with fixed AC port power, current of SM2 changes from -15 A to 0. Meanwhile, power supply of the AC port is changed from only the DC port to both BSMs and the DC port. The dc component I_{cir} of upper arm current i_u changes from 40 A to 34 A and current limits change to $I_{bau_max} = 16.7$ A and $I_{bau_min} = -35.7$ A. Current of SM1 is beyond the upper current limit before 0.6 s and within the limit after 0.6 s. Accordingly, capacitor voltages of BSMs within upper arm are imbalanced before 0.6 s and back in balance after 0.6 s.

C. Case III

This case is to verify the change of current limits with fixed $I_{cir} = 32$ A and changed I_{xarm} , in simulation. In this case, BSMs in the upper arm are the same as BSMs in the lower arm, and the upper arm is taken as an example to be analyzed.

Initially, as shown in Fig. 13, current of SM1 is set to 20 A and the other BSMs are set to zero. Peak value I_o of AC port

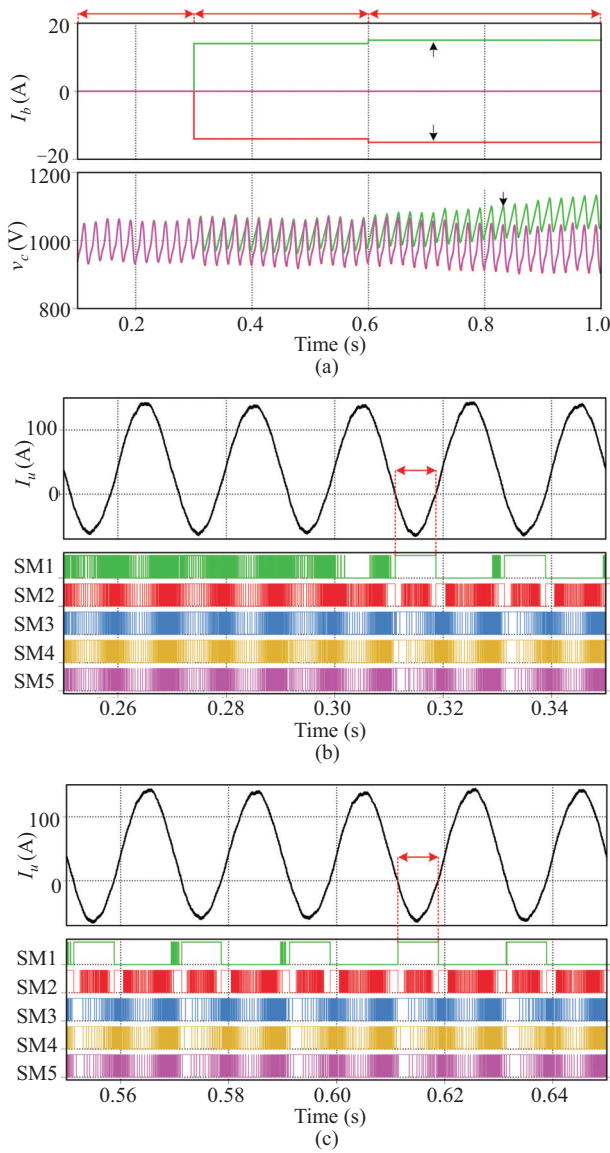


Fig. 11. Simulation results of current limits verification: (a) Voltages and currents of BSMs, (b) arm current and driving signals around 0.3 s, and (c) arm current and driving signals around 0.6 s.

current is 200 A and peak value $I_{u_{arm}}$ of the fundamental component of i_u is 100 A. I_{cir} is 32 A. Current limits are $I_{bau_max} = 17.5$ A and $I_{bau_min} = -34.4$ A. Current of SM1 is beyond the upper current limit and the capacitor voltage of SM1 deviates from the other BSMs.

At 0.3 s, AC current steps to $I_o = 280$ A. Currents of BSMs except SM1 step to 10 A to fully compensate the power increase of the AC port, which keeps I_{cir} at 32 A. Increase of I_o improves current limits to $I_{bau_max} = 29.7$ A and $I_{bau_min} = -40$ A. As currents of all BSMs are in the current limits, capacitor voltages of BSMs are rebalanced after 0.3 s.

V. EXPERIMENT VERIFICATION

A. Verification of Experiment Prototype

In order to carry out experimental verification of current limits, a downscaled experimental prototype of a single-phase

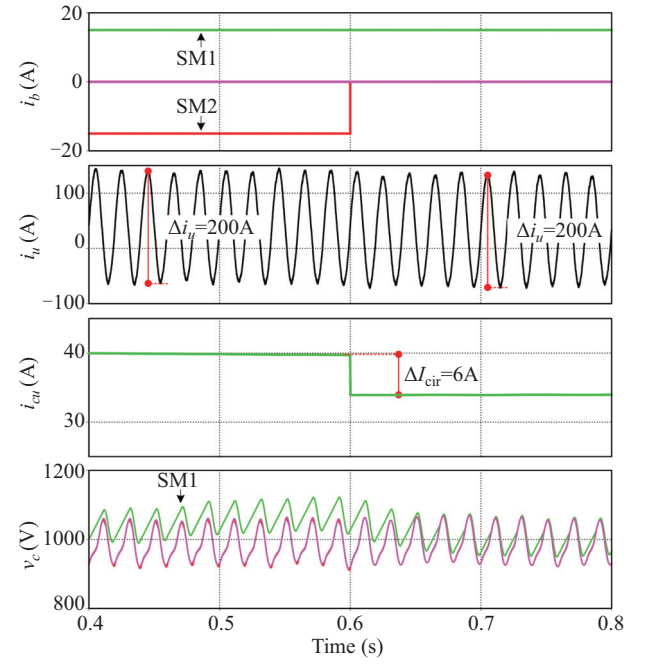


Fig. 12. Simulation waveforms with fixed I_{xarm} and changed I_{cir} .

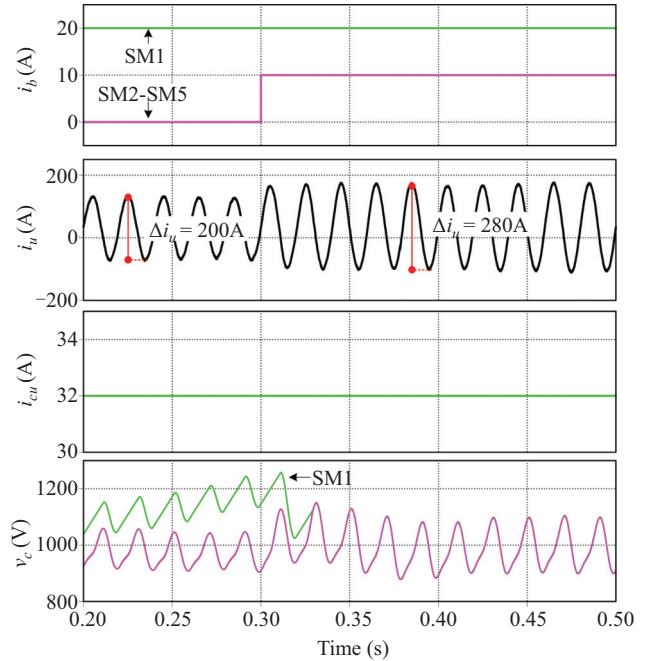


Fig. 13. Simulation waveforms with fixed I_{cir} and changed I_{xarm} .

MMC was built. The prototype platform is shown in Fig. 14, and prototype parameters are listed in Table III. The prototype uses a TMS320F28335 to implement the control strategy illustrated in Fig. 9.

As shown in Fig. 15, currents of SM1 and SM2 are 0.7 A and -0.7 A, respectively. The dc and fundamental frequency components of the arm current are 2.2 A and 5 A, and current limits are 0.65 A and -2.85 A. As SM1 current is beyond the upper limit, voltage of SM1 diverges as shown in Fig. 15(a).

Based on the operation condition in Fig. 15, peak value I_o of AC port current is enhanced and current of SM2 changes

TABLE III
PARAMETERS OF EXPERIMENTAL PROTOTYPE

Parameter	Value
DC voltage/ V_{dc} (V)	180
Capacitor voltage of SM/ V_c (V)	60
Number of SM/ N	3
Modulation index/ m	0.8
Arm inductor/ L_0 (mH)	6
AC side inductor/ L (mH)	6
BSM capacitance/ C (mF)	4

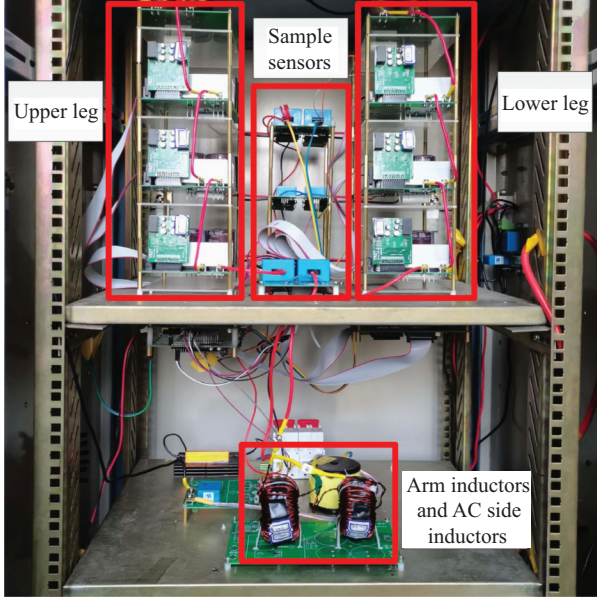


Fig. 14. Experimental prototype.

from -0.7 A to 0, simultaneously. Steady-state waveforms are shown in Fig. 16. Increase of the AC side power is fully compensated by decreased power of BSMs. In the meantime, DC port power keeps steady. The fundamental frequency component $I_{x_{arm}}$ of arm current increases to 6 A and dc component I_{cir} keeps at 2.2 A. Current limits are 0.94 A and -3.14 A. Current of SM1 is within current limits and capacitor voltages are back in balance as shown in Fig. 16(a). In Fig. 16(b), though SM1 still maintains insert-state during the period of $i_u < 0$, insert time of SM1 during $i_u > 0$ increases especially around the maximum i_u .

As shown in Fig. 17, peak value I_o of AC port current steps down from 16.3 A to 11.5 A, while currents of SM1 and SM2 maintain at 0.9 A and -0.9 A during the whole change period. As AC port current has significant influence on current limits, the upper current limit also steps down from 1.12 A to 0.78 A. Therefore, when the step-down of AC port current occurs, it is obvious voltages of SM1 and SM2 changes from balance to imbalance.

B. Experiment Verification of References

In this paper, [19] and [21] containing experimental results are used for testing validation of the current limits calculation method. Parameters needed for calculating the current limits, such as modulation index m , dc and fundamental frequency components of arm currents, submodule capacitor voltages, etc., are taken from their respective papers.

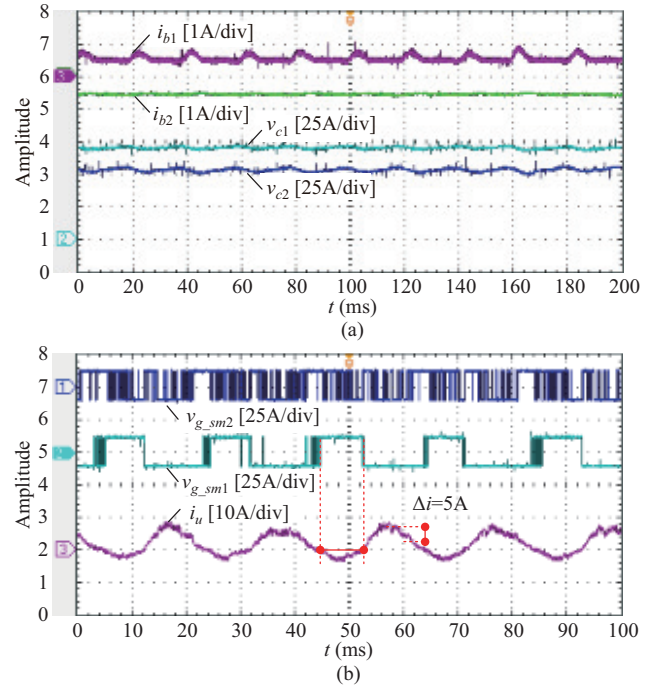


Fig. 15. Experimental waveforms of imbalanced capacitor voltage: (a) voltages and currents of SM1 and SM2, and (b) driving signals of SM1 and SM2, and arm current.

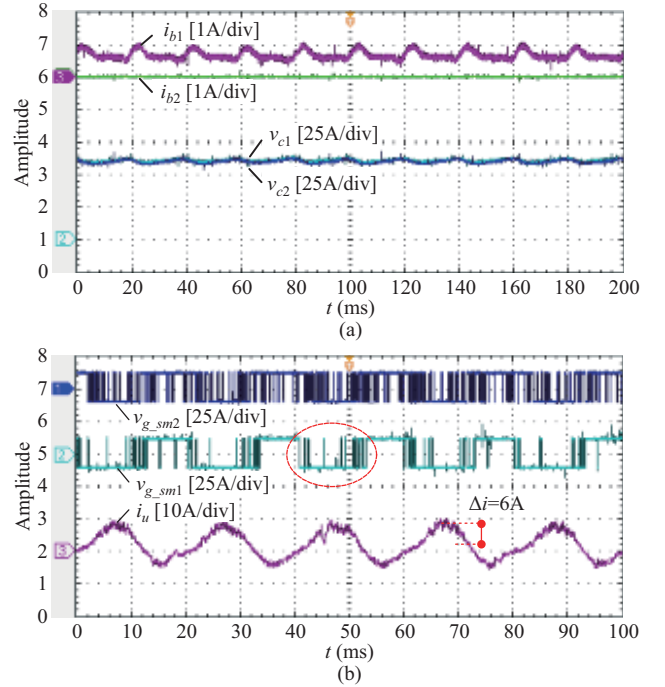


Fig. 16. Experimental waveforms of balanced capacitor voltage: (a) voltages and currents of SM1 and SM2, and (b) driving signals of SM1 and SM2 and arm current.

In [19], there are three experimental cases. Table IV shows the experimental parameters desired to calculate current limits and balanced results of the experiments and calculations.

Table V shows experimental maximum power limits results in [21] and power limits results calculated by the proposed method in this paper. In Table V, P_1^* represents maximum

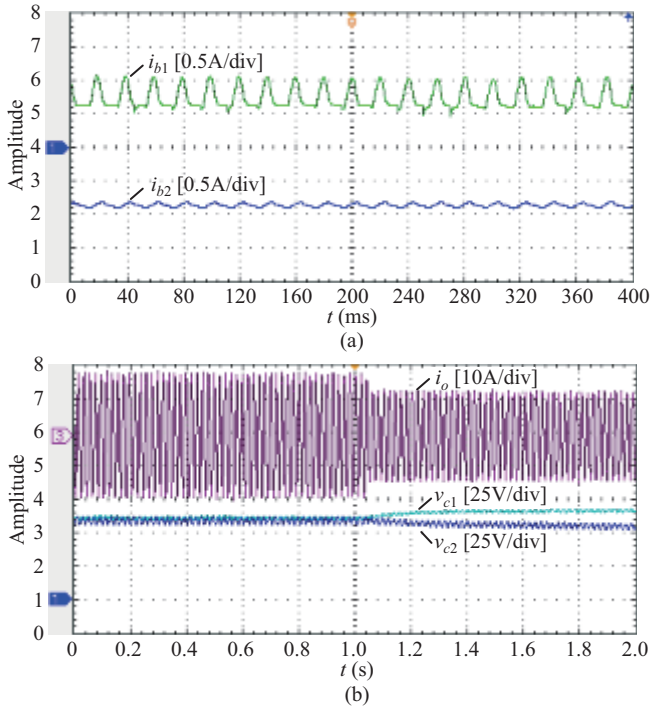


Fig. 17. Experimental waveforms of changing the AC side current: (a) currents of SM1 and SM2, and (b) ac side current and voltages of SM1 and SM2.

TABLE IV
PARAMETERS AND BALANCED RESULTS OF EXPERIMENTS IN [19] AND CALCULATIONS IN THIS PAPER

Parameters	Case 1	Case 2	Case 3
DC voltage/ V_{dc} (V)	920	920	920
DC current/ I_{dc} (A)	0	0	0
AC voltage(rms)/ V_o (V)	270	270	270
AC current(rms)/ I_o (A)	29.63	29.63	42.33
Number of SM per arm, N	4	4	4
Number of BSM	3	2	2
Power factor	1	1	0.7
Total active power/ P (kW)	8	8	8
Maximum current of SM (A)	5.8	8.7	8.7
Upper current limit (A)	6.67	6.67	9.53
Balanced results in [19]	Yes	No	Yes
Balanced results in this paper	Yes	No	Yes

TABLE V
EXPERIMENTAL RESULTS IN [21] AND CALCULATION RESULTS IN THIS PAPER

m	P_1^* PF = 1	P_2^* PF = 1	P_1^* PF = 0.827	P_2^* PF = 0.827
0.6	104.35%	106.1%	123.67%	128.3%
0.7	89.45%	90.95%	106.12%	109.9%
0.8	78.31%	79.6%	92.00%	96.22%
0.9	69.72%	70.7%	81.56%	85.53%

power limits in [21] and P_2^* is maximum power limits calculated in this paper. PF represents power factor.

In Table IV, results in [19] are consistent with results obtained by the proposed method in this paper. In Table V, calculation results in this paper are slightly larger than experimental results in [21].

In summary, it is concluded that the proposed current limits calculation method provides satisfactory results for judging the reasonability of current distribution on BSMs.

VI. CONCLUSION

On the basis of a general MMC-BESS and the basic principle of charge-discharge balance of capacitor, this paper proposes a method which utilizes the dc and fundamental frequency components of the arm current to calculate current limits. Current limits determine the limits of uneven power of batteries for maintaining balance of capacitor voltage. SMs within one arm respond to the same current limits. If all SM currents are in the current limits, capacitor voltage is balanced. On the opposite, even if only the current of one SM exceeds the current limits, capacitor voltage is unbalanced. Besides, the computational consumption of the proposed method is fixed and independent on the number of SM. According to analysis, current limits are enhanced with increase of the fundamental frequency component of the arm current. The sum of the upper limit and lower limit equals $-I_{cir}$, which facilitates calculation of current limits. In addition, the dc component determines the size relationship between absolute values of the upper and lower current limits. For verifying the theoretical analysis and current limits calculation method, both simulation model and experiment prototype were built and provide satisfactory results. Analysis and calculation of current limits, in this paper, contribute to a reasonable distribution of power on batteries in MMC-BESS for maintaining balance of capacitor voltage.

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